Customer No.: 31561
Docket No.: 11955-US-PA
Application No.: 10/708,371

REMARKS

This is a full and timely response to the outstanding nonfinal Office Action mailed Feb. 1, 2007. Applicants submit that claims 1, 7 and 13 have been amended hereby. Supports for the amendments to claims 1, 7, and 13 can be found throughout the specification and the drawings, specifically Figs. 3 and 7. Reconsideration and allowance of the application and presently pending independent claims 1, 7 and 13, as currently amended, and their dependent claims 2-6, 8-12, and 14-17, are respectfully requested.

Discussion of Office Action Rejections

Claims 1-17 were rejected under 35 U.S.C. 102(b) as being anticipated by Ishikawa et al. U.S. patent No. 5,982,236.

In response to the rejection to claims 1-17 under 35 U.S.C. 102(b) as being anticipated by Ishikawa et al., Applicants have amended claims 1, 7 and 13, and hereby otherwise traverses these rejection. As such, Applicant submits that claims 1-17 are now in condition for allowance.

Rejection Addressed To Claim 1

With respect to claim 1, as currently amended, recites in part:

A power amplifier with an active bias circuit, comprising:

...

an active bias circuit ***serially connected between an input power terminal of the power amplifier and the gate of the power amplifier transistor*** for

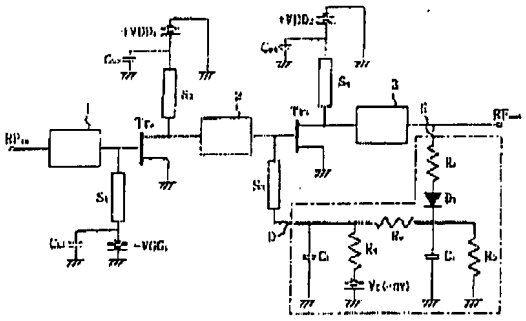
receiving an input power from the input power terminal and outputting the gate bias voltage to the gate, wherein ***the gate bias voltage is increased corresponding to an increase of the input power***, wherein the active bias circuit comprises ***a voltage source other than the input power***.

Applicant submits that such a power amplifier with an active bias circuit as set forth in claim 1, as amended, is neither taught, disclosed, nor suggested by Ishikawa et al. or any of the other cited references, taken alone or in combination.

Ishikawa et al. fails to disclose, teach or suggest "an active bias circuit ***serially connected between an input power terminal of the power amplifier and the gate of the power amplifier transistor*** for receiving an input power from the input power terminal and outputting the gate bias voltage to the gate, wherein ***the gate bias voltage is increased corresponding to an increase of the input power***, wherein the active bias circuit comprises ***a voltage source other than the input power***" (Emphasis added) that is required for the power amplifier, as set forth in claim 1, as amended. Therefore, claim 1, as currently amended, should not be considered as being anticipated by Ishikawa et al. or any of the other cited references, taken alone or in combination.

As shown in Fig. 17 of Ishikawa et al., up which the Office Action relied to anticipate claim 1,

Fig. 17
Prior Art



First, Ishikawa et al. fails to disclose, teach or suggest "an active bias circuit serially connected between an input power terminal of the power amplifier and the gate of the power amplifier transistor" as claimed in claim 1.

In addition, Ishikawa et al. fails to disclose, teach or suggest "the gate bias voltage is increased corresponding to an increase of the input power, wherein the active bias circuit comprises a voltage source other than the input power" as claimed claim 1.

It is stated in Col.3, Line 55 to Col.4, Line 5 of the Ishikawa et al., as followed:

> "The second conventional high-frequency power amplifier, as shown by a chain line in FIG. 17, comprises a negative bias voltage generation circuit connected with the output terminal of the output impedance matching circuit 3. The negative bias voltage generation circuit comprises a detection circuit for high-frequency power including a resistance R_1 and a diode D_1, and a voltage division circuit including a negative direct-current bias power

supply Vc (-5 V) and division resistances R_2, R_3, and R_4. The negative bias voltage generation circuit detects part of the high-frequency power which is outputted from the output impedance matching circuit 3 at a power detection point E, changes the direct-current bias voltage which is outputted from the negative **direct-current bias power supply Vc, based on the detected high-frequency power**, and outputs the direct-current bias voltage to the input terminal of the latter-stage transistor Tr_n from a negative bias voltage output point D via the third microstrip line S_3."

The asserted voltage source (Vc) in the Ishikawa et al. is changed based on the detected high-frequency power (E). However, as in the amended claim 1 of the invention, the voltage source other than the input power **does not depend on the input power**.

Thus, the Ishikawa et al. does not anticipate claim 1, and the rejection should be withdrawn.

If independent claim 1 is allowable over the prior art of record, then its dependent claims 2-6 are allowable as a matter of law, because these dependent claims contain all features of their respective independent claim 1. *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988). Additionally and notwithstanding the foregoing reasons for the allowability of claim 1, these dependent claims recite further features that are patentably distinct from the prior art of record.

Dependent claim 5 further recites the active bias circuit comprises a diode and a resistor. Dependent claim 6 further recites "an equivalent resistance of the diode in the active bias circuit varies in correspondence with the input power."

As stated in Col.4, Lines 20-31 of the Ishikawa et al., as followed:

> "…. the second conventional high-frequency power amplifier also has a drawback. The peripheral circuit has a negative direct-current bias power supply V_c, and for the negative direct-current bias power supply V_c to generate negative voltage of around -5 V, it is necessary to provide a negative voltage generation circuit which generates negative voltage based on the positive voltage outputted from the positive power supply $+VDD_2$. Since the negative voltage generation circuit is constantly supplied with a current of 10 mA, the second conventional high-frequency power amplifier fails to reduce the current consumption when the entered high-frequency power is small."

The high-frequency power amplifier as disclosed in FIG.17 of the Ishikawa et al. has the drawback that the negative direct-current bias power supply V_c to generate negative voltage, it is necessary to provide a negative voltage generation circuit which generates negative voltage based on the positive voltage outputted from the positive power supply, which fails to reduce the current consumption when the entered high-frequency power is small.

However, as claimed in claim 1 and further in claims 5 and 6 of the invention, the voltage source **does not change based on the input power**, instead, the equivalent resistance of the diode in the active bias circuit varies in correspondence with the input power, which makes "***the gate bias voltage being increased corresponding to an increase of the input power***" as claimed in claim 1 and further in claims 5 and 6.

Thus, the Ishikawa et al. does not anticipate claims 5 and 6, and the rejection should be withdrawn.

Rejection Addressed To Claims 7 and 13

Claim 7, as currently amended, recites in part:

An integrated circuit for a power amplifier with an active bias circuit, comprising:

a power output device, from which a power is received for the power amplifier operation;

...

an active bias circuit serially connected between the power output device and the gate of the power amplifier transistor for receiving an input power from the power output device and providing a gate bias voltage to the gate, wherein the gate bias voltage is increased corresponding to an increase of the input power, wherein the active bias circuit comprises ***a voltage source other than the input power***;

...

Likewise, claim 13, as currently amended, recites in part:

A method for generating a gate bias voltage of a power amplified transistor corresponding to an input power, comprising:

providing an input power ***to an active bias circuit disposed before the power amplified transistor***;

...

wherein the input power is transmitted along a path constituting of a first terminal from which the input power is inputted, the active bias circuit, the power amplified transistor, a terminal from which the gate bias voltage is outputted in that sequence.

For similar reasons, Ishikawa et al. fails to disclose, teach or suggest "a power output device, **from which a power is received for the power amplifier operation**" and "an active bias circuit **serially connected between the power output device and the gate of the power amplifier transistor**" that is required by claims 7, as currently amended (Emphasis added); Ishikawa et al. still fails to disclose, teach or suggest "providing an input power **to an active bias circuit disposed before the power amplified transistor**", and "**wherein the input power is transmitted along a path constituting of a first terminal from which the input power is inputted, the active bias circuit, the power amplified transistor, a terminal from which the gate bias voltage is outputted in that sequence**" that is required by claim 13 as currently amended (Emphasis added).

Accordingly, the present invention as set forth in claims 7, and 13, and their dependent claims 8-12, and 14-17 are novel and unobvious over Ishikawa et al., and thus should be allowable.

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CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

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